Introduction to VME / VXI / VXS Standards

ANSI VITA VME Standard (VME32/VME64)

VME bus is a computer bus standard, originally developed for the Motorola 68000 line of CPUs, but later widely used for many applications and standardized by the IEC as ANSI/IEEE 1014-1987. It is physically based on the Eurocard sizes, mechanics and connectors, but uses its own signaling system. It was first developed in 1981 and continues to see widespread use today.

Since it's creation 25 years ago the original VME bus standard has seen a number of extensions and add-ons.

Year	Standard	Features	Page
1982	**VME32 rev.A**	32bit parallel bus, A32, D32 max 40MB/s 3 row DIN connectors P1, P2	22
1987	**ANSI/IEEE 1014-1987**	Standard adopted based on VME Rev. C	22
1987	**VXI**	VME extension for instrumentation	25
1990	**VME430**	CERN nuclear VME 30 pin P_{aux} connector additional -5.2V, -2V, +/-15V	28
1982	**VME64**	Multiplexed 64 bit, A64, D64 max 80MB/s	22
1996	**VME64x**	New 160 pin connectors, metric P0 connector EMC, ESD (IEEE 1101.10) additional +3.3V (opt. 48V)	29
1998	**VME64xP**	VIPA (Physics), redefined P0 add. 9U x 400mm size	30
2003	**VME 2eSST**	Up to 320MB/s	30
2003	**VXS**	Serial high speed fabric (P0)	31

History

In 1979 Jack Kister and John Black, engineers at Motorola, began creating a new processor bus system to go with the MC68000 CPU. As more designers became involved and the system was further refined, it later became known as the VME bus.

The new VME bus had many advantages and was soon adopted as a standard for a number of other companies that were involved with the Motorola 68000. The first Official VME bus standard was released by the IEC as IEC 821 and by ANSI and IEEE as ANSI/IEEE 1014-1987. Development continues today primarily driven by the VME International Trade Association (VITA).

VME originally featured a 24-bit address bus and 16-bit data bus. Several updates to the system allow wider bus widths. The current **VME64** standard defines a full 64-bit bus in 6U-sized cards and 32-bit in 3U cards. The VME64 protocol has a maximum data transfer rate of 80 MByte/s.

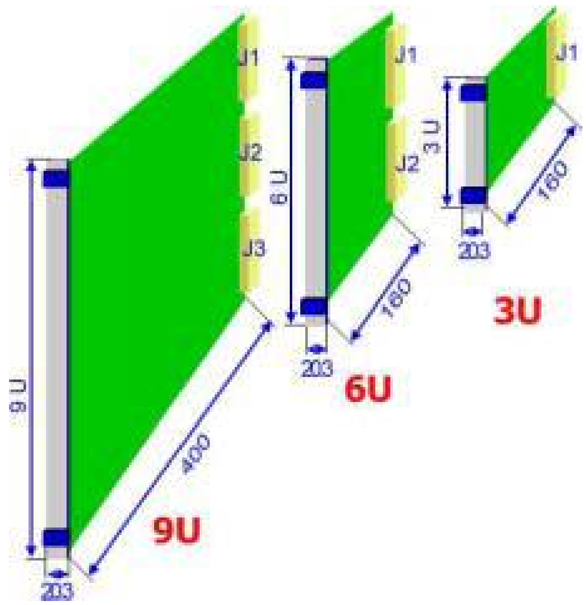
In the late 1990's, VITA defined synchronous protocols to improve the data transfer bandwidth on existing VME64 backplanes. A new 2eSST protocol was approved in ANSI/VITA 1.5 in 1999, which allows up to 320 Mbytes/s.

Many extensions have been added to the VME interface, providing 'sideband' channels of communication in parallel to VME itself. Some examples are IP Module, RACEway Interlink, SCSA, Gigabit Ethernet on VME64x Backplanes, PCI Express, RapidIO, StarFabric and InfiniBand and VXI.

VME is a multi-master bus. A bus arbiter, in the left-most slot (slot 1) determines which of several competing masters acquires the bus. Arbitration can be prioritized with 7 bus request levels or round robin. VME also defines a flexible prioritized interrupt subsystem.

Hardware Description

VME card mechanical dimensions meet the Eurocard Standard. The connection between the module and the backplane is made by two 96-pin DIN 41612 connectors. The number of connectors used determines the address space of the card and the card size. Uncommitted pins on the connectors provide support for application specific busses and rear transition modules. 9-U modules may provide a third connector for application specific use.



VME card sizes and connector positions

VME modules come in three sizes. 3U x160mm cards have one backplane connector (J1) and have a 24-bit/16-bit address/data space. 6U x 160mm cards are the most common ones and have two backplane connectors (J1 & J2) allowing for 32 bits of address/data space. Large 9U x 400mm cards also have 32 address/data lines and 2 connectors (J1 & J2).

Each VME card is 20.3mm wide. Twenty-one cards will fit into a 19 rack mounted VME crate.

VME crates, or chassis, provide the mechanical support with card guides and the VME bus backplane into which the modules are plugged. The crate typically has a power supply, which provides power to the backplane. Standard VME voltages are **5V and +/-12V**. For proper cooling the crate should be outfitted with a cooling fan or fan tray.

Bus Description

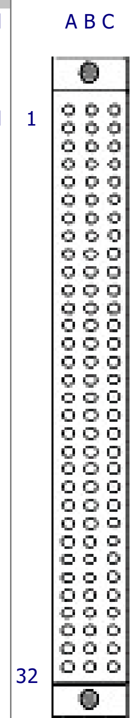
Address Lines

The VME bus has 31 address lines. The first 23 lines are present on J1 and the remainder being on J2. The lowest address bit (A0) is implied by the transfer cycle and is not present on the backplane. VME64 can multiplex address and data lines allowing 31 address bits on J1 and an additional 32 address bits on J2.

Data Lines

The VME bus has 32 data lines. The low order 16 data lines are on J1, the high order 16 on J2. VME modules with only J1 can only do 16 bit wide transfers, while those with both J1 and J2 can do 32 bit wide transfers. VME64 modules multiplex address and data allowing 32 bit transfers on J1, and 64 bit wide transfers when both connectors are present.

Pin No.	J1/P1 (top)			J2/P2 (bottom)		
	Row A	Row B	Row C	Row A	Row B	Row C
01	D00	BBSY*	D08	User defined	+5 V	User defined
02	D01	BCLR	D09	User defined	GND	User defined
03	D02	ACFAIL*	D10	User defined	Reserved	User defined
04	D03	BG0IN*	D11	User defined	A24	User defined
05	D04	BG0OUT*	D12	User defined	A25	User defined
06	D05	BG1IN*	D13	User defined	A26	User defined
07	D06	BG1OUT*	D14	User defined	A27	User defined
08	D07	BG2IN*	D15	User defined	A28	User defined
09	GND	BG2OUT*	GND	User defined	A29	User defined
10	SYSCLK	BG1IN*	SYSFAIL*	User defined	A30	User defined
11	GND	BG3OUT*	BERR*	User defined	A31	User defined
12	DS1*	BR0*	SYSRESET*	User defined	GND	User defined
13	DS0*	BR1*	LWORD*	User defined	+5 V	User defined
14	WRITE*	BR2*	AM5	User defined	D16	User defined
15	GND	BR3*	A23	User defined	D17	User defined
16	DTACK*	AM0	A22	User defined	D18	User defined
17	GND	AM1	A21	User defined	D19	User defined
18	AS*	AM2	A20	User defined	D20	User defined
19	GND	AM3	A19	User defined	D21	User defined
20	IACK*	GND	A18	User defined	D22	User defined
21	IACKIN*	SERCLK	A17	User defined	D23	User defined
22	IAOUT*	SERDAT	A16	User defined	GND	User defined
23	AM4	GND	A15	User defined	D24	User defined
24	A07	IRQ7*	A14	User defined	D25	User defined
25	A06	IRQ6*	A13	User defined	D26	User defined
26	A05	IRQ5*	A12	User defined	D27	User defined
27	A04	IRQ4*	A11	User defined	D28	User defined
28	A03	IRQ3*	A10	User defined	D29	User defined
29	A02	IRQ2*	A09	User defined	D30	User defined
30	A01	IRQ1*	A08	User defined	D31	User defined
31	-12 V	+5V STDBY	+ 12 V	User defined	GND	User defined
32	+5 V	+ 5 V	+ 5 V	User defined	+ 5 V	User defined



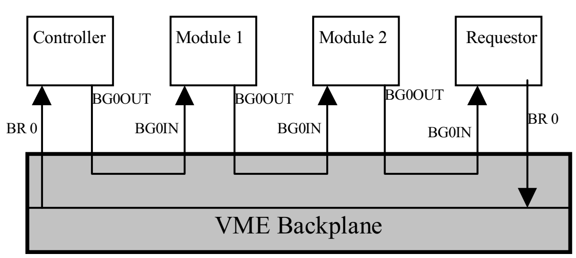
DIN 41612
96-pin

VME Backplane connectors and pin layout

Bus Arbitration

A VME Bus master requests the bus by asserting one of the bus request lines BR0*-BR3*. The slot 1 bus arbiter (some masters include bus arbitration logic) will grant the bus by asserting the corresponding bus grant signal (BG0OUT-BG3OUT). The arbiter can cyclically scan the BRn* lines (round robin arbitration), or treat higher numbered BRn* lines as being a higher priority request (prioritized arbitration).

The bus grant forms a daisy chain. Each module monitors BG0IN-BG3IN if it is not requesting the bus it reproduces these signals on BG0OUT-BG3OUTwhich are inputs to the next slot to the right on the backplane. If the module is requesting the bus on the corresponding BRn* it claims the bus by driving BBSY*.



Bus request and grant daisy chain

Data Strobe Lines

DS0* and DS1* are tri-state signals used in conjunction with LWORD* to indicate how many byte locations are being accessed (1, 2, 3, or 4). For byte transfers these signals imply bit zero of the address. During a write cycle, the falling edge of the first data strobe indicates that valid data is available on the data bus. For read cycles, the rising edge of the first data strobe indicates that data has been accepted from the Addressed slave.

Address Strobe Line

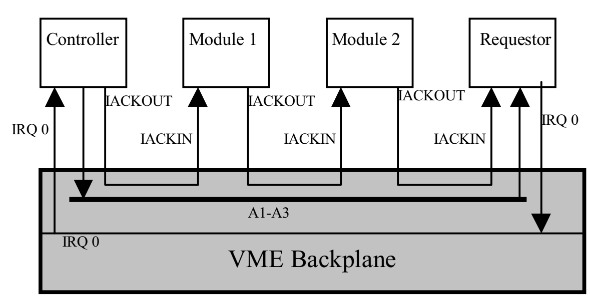
The Address strobe Line (AS*) is driven low by a master to indicate it is driving a valid address.

Data Acknowledge Line

DTACK* is an open-collector signal generated by slaves. The falling edge of this signal indicates that valid data is available on the data bus during a read cycle, or that the slave has accepted data during a write cycle. The rising edge of DTACK indicates when the slave's data is no longer present at the end of a read cycle.

Interrupt Handling

Any module on the VME bus may request an interrupt by driving one of the interrupt request lines IRQ1*-IRQ7*. Any bus master module can respond to any of the interrupt request lines by arbitrating for the bus, asserting IACK* and echoing the interrupt level on A1-A3. The bus arbiter places the IACKOUT* on an interrupt daisy chain (similar to the bus grant daisy chain). The interrupting module will then provide a *status-id* on the data bus that allow the interrupt handler to distinguish between interrupters sharing the same interrupt request level.



VME Interrupt handling

Clock
SYSCLK is a totem pole signal that provides a constant 16 MHz clock signal from the system controller.

System Fail Line
The SYSFAIL* line is an open-collector signal that indicates when a failure has occurred in the system. Any board in the system can generate this signal.

System Reset
The SYSRESET requests that all bus modules perform power-up initialization.

Write Line
WRITE* is a three-state signal generated by the master to indicate whether the data transfer cycle is a read or write. A high level indicates a read operation; a low level indicates a write operation.

Address Modifiers
VME provides for large number of data transfer types. The VME Address modifier lines (AM0*-AM5*) are asserted by a bus master during an address cycle to indicate the type of data transfer requested.

AM	Address	Description
0x3F	24	A24 supervisory block transfer (BLT)
0x3E	24	A24 supervisory program access
0x3D	24	A24 supervisory data access
0x3C	24	A24 supervisory 64-bit block transfer (MBLT)
0x3B	24	A24 non-privileged block transfer (BLT)
0x3A	24	A24 non-privileged program access
0x39	24	A24 non-privileged data access
0x38	24	A24 non-privileged 64-bit block transfer, MBLT
0x37	40	A40BLT [MD32 data transfer only]
0x35	40	A40 lock command (LCK)
0x34	40	A40 access
0x32	24	A24 lock command (LCK)
0x2F	24	CR / CSR space
0x2D	16	A16 supervisory access
0x2C	16	A16 lock command (LCK)
0x29	16	A16 non-privileged access
0x21	32/64	2eVME for 3U bus modules (address size in XAM code)
0x20	32/64	2eVME for 6U bus modules (address size in XAM code)
0x0F	32	A32 supervisory block transfer (BLT)
0x0E	32	A32 supervisory program access
0x0D	32	A32 supervisory data access
0x0C	32	A32 supervisory 64-bit block transfer (MBLT)
0x0B	32	A32 non-privileged block transfer (BLT)
0x0A	32	A32 non-privileged program access
0x09	32	A32 non-privileged data access
0x08	32	A32 non-privileged 64-bit block transfer MBLT
0x05	32	A32 lock command (LCK)
0x04	64	A64 lock command (LCK
0x03	64	A64 block transfer (BLT)
0x01	64	A64 single access transfer
0x00	64	A64 64-bit block transfer (MBLT)

List of VME address modifiers

Long Word
The LWORD* line is used in conjunction with DS0*, DS1*, to specify the width of a data transfer.

Serial Data
The SERCLK and SERDAT lines implement a serial data bus. SERCLK provides a synchronization clock for the serial data that can be transferred on SERDAT.

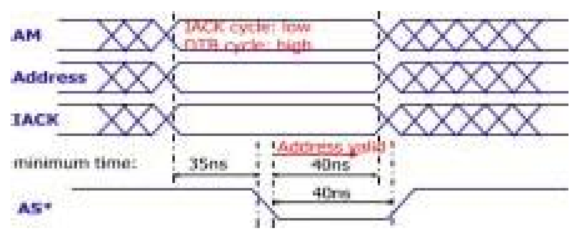
Bus Busy and Bus Clear
The master that has been granted the bus assert BBSY* to indicate the bus is in use. In priority arbitration, the bus arbiter can assert BCLR* if a bus request at a higher priority than the currently granted master is present. The current bus master is then expected to release the bus when convenient by releasing BBSY, to allow the new arbitration cycle to complete.

AC FAIL
The ACFAIL line is driven low when there is an AC failure for the VME power supply.

Bus Errors
The bus arbiter often implements address timeout logic and asserted BERR* if no module responds to an address cycle within the timeout. Slaves may also assert BERR* if they are not able to honor a requested cycle (e.g. they do not support the requested address modifier).

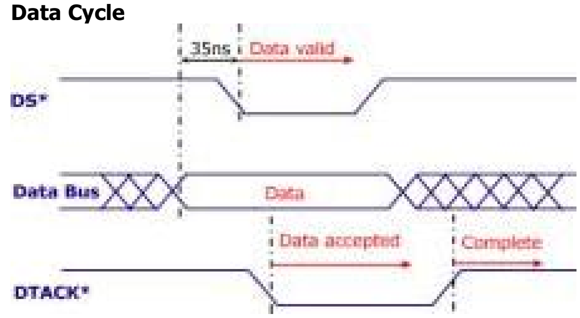
VME Bus Timing

Address Cycle



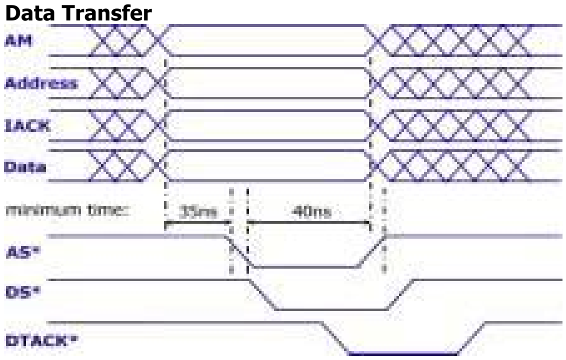
During an address cycle, a VME bus master holds IACK high and places the address and AM [0-5] codes on the bus. Once the lines have been valid for at least 35ns the Master drives the Address Strobe [AS*] indicating a valid address is on the bus. For interrupt acknowledge cycles the IACK line is driven low, the interrupt priority is encoded on A1-A3 and the AM lines are ignored.

Data Cycle



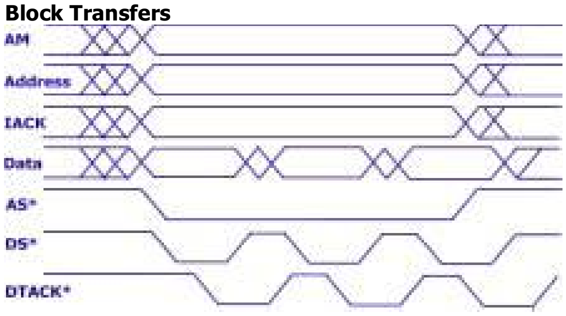
VME Data cycles can be writes (Master to Slave) or reads (Slave to Master). Regardless of the cycle type, the Master uses LWORD*, DS0* and DS1*to indicate the width of the transfer. At least one of DS0*, DS1* will be driven. For a write cycle, DS0* and DS1* also indicate that the Master has stable data on the data bus for the slave. In a read cycle, DS0* and DS1* indicate the master is ready to receive data from the slave. In a write cycle, DTACK* is asserted by the slave when it has accepted the data transfer. In a read cycle DTACK* indicates the slave has stable data on the bus for the master. Regardless of the cycle type, the release of both DS0* and DS1*, and subsequent release of DTACK* by the slave indicates completion of the cycle.

Data Transfer



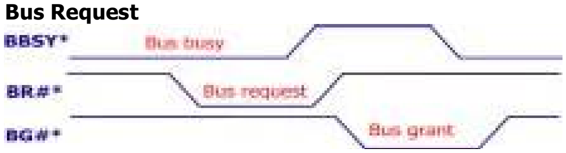
Data transfer requires an address and a data cycle. Address cycles may overlap the previous data cycle.

Block Transfers



A VME bus BLock Transfer [BLT] consists of a single Address cycle followed by up to 256 bytes of Data transfer before another address cycle is required. VME64 adds the Multiplexed Block Transfer [MBLT]. MBLT transfer data on both the address and data lines to achieve a 64 bit transfer width.

Bus Request



The master requesting the bus does so by driving a Bus Request (BR#*) line low. The VME bus arbiter hands control of the bus to a master by asserting the corresponding BG#* line.

VXI Standard (IEEE 1155)

The **VXI bus** architecture is an open standard platform for automated test instruments based upon VMEbus, the Eurocard standards, and other instrumentation standards such as IEEE-488.2. VXI's core market is in Telcecommunication, Military and Aerospace automatic test systems and data acquisition applications.

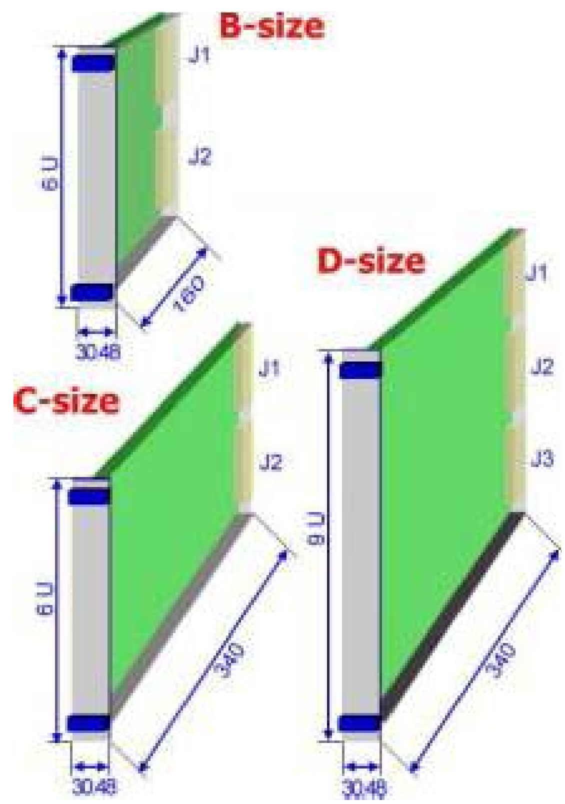
The original standard for "**V**ME e**X**tensions for **I**nstrumentation System Specification" **VXI-1 Revision 1** was introduced in August 1987 by the VXI Bus Consortium which included companies as Colorado Data Systems, Hewlett-Packard, Racal Dana, and Tektronix. Revision 3 added VME64 64-bit transfers and features. The VXI-1 specification has been adopted by the IEEE as IEEE Std 1155-1992. For more information see http://www.vxibus.org/.

VXI implements the VME bus protocol for data transfers between modules but implements a number of significant enhancements towards data acquisition and automated test applications. Especially the VXI mechanical and power supply specifications provide an excellent electrical environment for low-level, high accuracy analog circuitry.

- Larger card size to increase VXI board space, provides space for sophisticated analog circuits, signal conditioning and better analog to digital isolation
- 1.2" module spacing, fully shielded mechanical design of modules to minimize noise pickup and provides more front panel space,
- 3 different module sizes (B, C, D-size)
- Mandatory analog power supply voltages (-5.2V, -2V, +/-24V) and strict limits for power supply noise
- Specifications for cooling and measurement of cooling performance (VXI-8) to allow use of high power electronic circuits in VXI modules.
- VXI Backplane provides precision clocks and trigger lines for common clocking and triggering / event handling across VXI modules
- Geographic addressing, dynamic address allocation
- Local bus for inter-module communication
- Power-up self test (status register bit indicates whether the module passed self-test or not).
- Definition of module standard registers including: manufacturer ID, Serial Number, Module Hardware / Firmware Revision Level

VXI System and Sub-system

A VXI bus system can have up to 256 devices, including one or more VXI bus subsystems. A VXI bus subsystem consists of a central timing /controller module in Slot 0 (*Slot-0 controller)* with up to twelve additional instrument modules. The Slot 0 module is responsible for managing system resources such as the VXI bus mandated timing generation, the VME bus system controller functions and a possible data communication ports such as Ethernet, RS232 or IEEE 488.



A typical **VXI crate** has 13 slots (numbered 0 through 12 from the left as viewed from the front). The VXI crate has provides power for the following DC voltages:

+5V, +/-12V (as per VME spec.),
-5.2V, -2V (for ECL devices / termination),
+/-24V (for analog circuits)

Maximum allowed power supply DC noise levels at 10MHz bandwidth are $50mV_{pp}$ with the exception of +/-24V line ($150mV_{pp}$). All WIENER VXI crates have lowest noise power supplies with $<10mV_{pp}$.

To guarantee proper cooling of all plugged in modules the VXI crate has to be outfitted with a fan tray. The provided airflow and distribution has to comply with VXI-8 specification.

There are 3 sizes of VXI modules: B, C and D. B-size modules are the same size as standard 6U VME modules and have identical 96-pin DIN connectors P1 and P2. Most popular is the C-size with the same 6U height but 340mm deep modules. The D-size module is a triple height Eurocard (9U) and can be outfitted with an additional P3 connector, which requires a special 9U backplane.

The VXI backplane for B- and C-size applications is a 6U high monolithic backplane with 13 slots. The pin layout is identical to VME for the top J1 connector as well as the center row of the lower J2 connector.

On the J2/P2 outer A and C rows (not used by VME) VXI adds a 10 MHz ECL clock, ECL and TTL trigger lines, an analog summing bus, a module identification line, the local bus and additional DC voltages:

- -5.2 V, -2 V, ±24 V and additional +5 V power
- 10 MHz differential clock
- 2 parallel ECL trigger lines
- 8 parallel TTL trigger lines
- 12 lines of defined local bus (daisy chain)
- 50 Ω terminated analog summing bus
- Module identification pin

VXI D-sized modules have a third connector J3/P3 on the bottom of the 9U high backplane. This J3/P3 connector adds of the similar resources as J2/P2. To support higher performance instrumentation it also includes a 100 MHz clock and sync signal as well as high precision star" trigger system where ECL trigger signals are routed through Slot 0 acting as a cross point switch. Further 24 additional lines of daisy chain local bus are defined on P3/J3.

- Additional +5V, -5.2V, -2V, ±24V and ±12V power.
- 100 MHz differential clock (synchronous with CLK10)
- Synchronizing signal for 100 MHz clock edge selection
- 4 additional ECL trigger lines, (total of 6)
- 24 additional local bus lines (total of 36)
- Star Trigger lines for precision module to module timing

CLK10 - Differential Clock
CLK10 is a 10 MHz system clock. It is sourced from Slot 0 and distributed to Slots 1-12 on P2. The Slot 0 output is differential ECL, which is buffered on the backplane and distributed to each module slot as a single source, single destination differential ECL signal.

CLK100 – Differential Clock (D-size only)
CLK100 is a 100 MHz system clock distributed via J3/P3. It is sourced from Slot 0, buffered on the backplane and distributed to each module slot as a single source, single destination differential ECL signal. Distribution delays have to be matched to provide a tight timing relationship between modules. CLK100 has to be synchronous to CLK10.

Pin No.	J2/P2 (SLOT 0) Row A	Row B	Row C
01	ECLTRG0	+5 V	CLK10+
02	-2 V	GND	CLK10-
03	ECLTRG1	Reserved	GND
04	GND	A24	-5.2 V
05	LBUSA00	A25	LBUSC00
06	LBUSA01	A26	LBUSC01
07	-5.2 V	A27	GND
08	LBUSA02	A28	LBUSC02
09	LBUSA03	A29	LBUSC03
10	GND	A30	GND
11	LBUSA04	A31	LBUSC04
12	LBUSA05	GND	LBUSC05
13	-5.2 V	+5 V	-2 V
14	LBUSA06	D16	LBUSC06
15	LBUSA07	D17	LBUSC07
16	GND	D18	GND
17	LBUSA08	D19	LBUSC08
18	LBUSA09	D20	LBUSC09
19	-5.2 V	D21	-5.2 V
20	LBUSA10	D22	LBUSC10
21	LBUSA11	D23	LBUSC11
22	GND	GND	GND
23	TTLTRG0*	D24	TTLTRG1*
24	TTLTRG2*	D25	TTLTRG3*
25	+5 V	D26	GND
26	TTLTRG4*	D27	TTLTRG5*
27	TTLTRG6*	D28	TTLTRG7*
28	GND	D29	GND
29	RSV2	D30	RSV3
30	MODID	D31	GND
31	GND	GND	+24 V
32	SUMBUS	+ 5 V	-24 V

A B C
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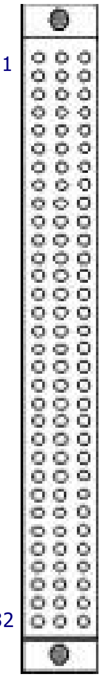
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DIN 41612
96-pin

J2/P2 Pin Layout (Slot 0)

Pin No.	J2/P2 (SLOT 1-12) Row A	Row B	Row C
01	ECLTRG0	+5 V	CLK10+
02	-2 V	GND	CLK10-
03	ECLTRG1	Reserved	GND
04	GND	A24	-5.2 V
05	LBUSA00	A25	LBUSC00
06	LBUSA01	A26	LBUSC01
07	-5.2 V	A27	GND
08	LBUSA02	A28	LBUSC02
09	LBUSA03	A29	LBUSC03
10	GND	A30	GND
11	LBUSA04	A31	LBUSC04
12	LBUSA05	GND	LBUSC05
13	-5.2 V	+5 V	-2 V
14	LBUSA06	D16	LBUSC06
15	LBUSA07	D17	LBUSC07
16	GND	D18	GND
17	LBUSA08	D19	LBUSC08
18	LBUSA09	D20	LBUSC09
19	-5.2 V	D21	-5.2 V
20	LBUSA10	D22	LBUSC10
21	LBUSA11	D23	LBUSC11
22	GND	GND	GND
23	TTLTRG0*	D24	TTLTRG1*
24	TTLTRG2*	D25	TTLTRG3*
25	+5 V	D26	GND
26	TTLTRG4*	D27	TTLTRG5*
27	TTLTRG6*	D28	TTLTRG7*
28	GND	D29	GND
29	RSV2	D30	RSV3
30	MODID	D31	GND
31	GND	GND	+24 V
32	SUMBUS	+ 5 V	-24 V

A B C
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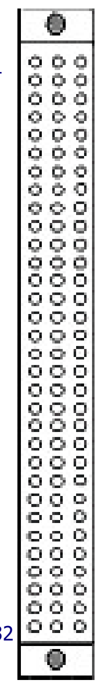
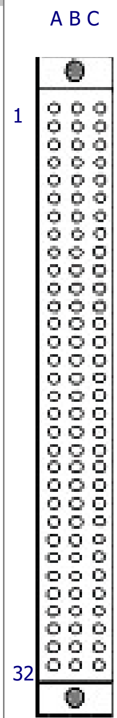

32
DIN 41612
96-pin

J2/P2 Pin Layout (Slot 1-12)

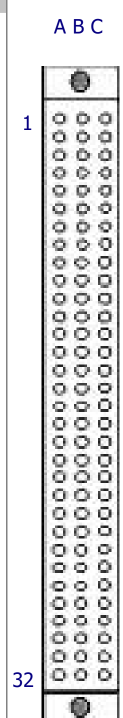
Pin No.	J3/P3 (SLOT 0) Row A	Row B	Row C
01	ECLTRG2	+24 V	+12 V
02	GND	-24 V	-12 V
03	ECLTRG3	GND	RSV4
04	-2 V	RSV5	+5 V
05	ECLTRG4	-5.2 V	RSV6
06	GND	RSV7	GND
07	ECLTRG5	+5 V	-5.2 V
08	-2 V	GND	GND
09	STARY12+	+5 V	STARX01+
10	STARY12-	STARY01-	STARX01-
11	STARY12+	STARY12-	STARX01+
12	STARY11+	GND	STARX02+
13	STARY11-	STARY02-	STARX02-
14	STARY11+	STARY11-	STARX02+
15	STARY10+	+5 V	STARX03+
16	STARY10-	STARY03-	STARX03-
17	STARY10+	STARY10-	STARX03+
18	STARY09+	-2 V	STARX04+
19	STARY09-	STARY04-	STARX04-
20	STARY09+	STARY09-	STARX04+
21	STARY08+	GND	STARX05+
22	STARY08-	STARY05-	STARX05-
23	STARY08+	STARY08-	STARX05+
24	STARY07+	+5 V	STARX06+
25	STARY07-	STARY06-	STARX06-
26	STARY07+	STARY07-	STARX06+
27	GND	GND	GND
28	STARY+	-5.2 V	STARY+
29	STARY-	GND	STARY-
30	GND	-5.2 V	-5.2 V
31	CLK100+	-2 V	SYNC100+
32	CLK 100-	GND	SYNC100-



DIN 41612
96-pin

J3/P3 Pin Layout (Slot 0)

Pin No.	J3/P3 (SLOT 1 – 12) Row A	Row B	Row C
01	ECLTRG2	+24 V	+12 V
02	GND	-24 V	-12 V
03	ECLTRG3	GND	RSV4
04	-2 V	RSV5	+5 V
05	ECLTRG4	-5.2 V	RSV6
06	GND	RSV7	GND
07	ECLTRG5	+5 V	-5.2 V
08	-2 V	GND	GND
09	LBUSA12	+5 V	LBUSC12
10	LBUSA13	LBUSC15	LBUSC13
11	LBUSA14	LBUSA15	LBUSC14
12	LBUSA16	GND	LBUSC16
13	LBUSA17	LBUSC19	LBUSC17
14	LBUSA18	LBUSA19	LBUSC18
15	LBUSA20	+5 V	LBUSC20
16	LBUSA21	LBUSC23	LBUSC21
17	LBUSA22	LUBSA23	LBUSC22
18	LBUSA24	-2 V	LBUSC24
19	LBUSA25	LBUSC27	LBUSC25
20	LBUSA26	LBUSA27	LBUSC26
21	LBUSA28	GND	LBUSC28
22	LBUSA29	LBUSC31	LBUSC29
23	LBUSA30	LBUSA31	LBUSC30
24	LBUSA32	+5 V	LBUSC32
25	LBUSA33	LBUSC35	LBUSC33
26	LBUSA34	LBUSA35	LBUSC34
27	GND	GND	GND
28	STARX+	-5.2 V	STARY+
29	STARX-	GND	STARY-
30	GND	-5.2 V	-5.2 V
31	CLK100+	-2 V	SYNC100+
32	CLK100-	GND	SYNC100-



DIN 41612
96-pin

J3/P3 Pin Layout (Slot 1 - 12)

ECLTRG0-5 - ECL Trigger lines

The 6 ECLTRG lines (C-size:0, 1 only) are used as an inter-module timing resource and can be accessed by any VXI module. These lines are single-ended ECL with 50 ohm impedance (terminated with 50Ω to -2 V on backplane). ECLTRG lines have a set of defined protocols corresponding to the TTLTRG* protocols.

LOCAL BUS

The Local Bus is a daisy chained bus structure with 36 lines (C-size:12 lines only) which allows several types of signal levels to be transmitted via this bus. For protection a keying mechanism is provided. The Local Bus key provides support for TTL, ECL and analog communication.

Number	Class	Range
1	TTL	-0.5 V ... +5.5 V
2	ECL	-5.46 V ... 0.0 V
3	ANALOG LOW	-5.5 V ... +5.5 V
4	ANALOG MED	-16.0 V ... +16.0 V
5	ANALOG HIGH	-42.0 V ... +42.0 V
6	RESERVED	

TTLTRG0-7* - TTL Trigger Lines

These open collector TTL lines are used for inter-module communication as trigger, handshake, clock or logic state transmission. Any module, including Slot 0, can drive these lines and receive information on these lines. Some standard allocation procedures and protocols as synchronous (SYNC), asynchronous (ASYNC) and start/stop (STST) are defined.

SUMBUS

The SUMBUS is an analog summing node that is bussed on the VXI backplane. Any module can drive it via an analog current source or receive from this line using a high impedance receiver. The SUMBUS is terminated to ground through 50ohm on both ends of the backplane.

STARX and STARY

Bi-directional STAR trigger lines provide inter-module asynchronous communication. Two STAR lines are connected between each module slot and Slot 0. Slot 0 may provide a cross-point switch that can be programmed to route signals between any two STARX or STARY lines. It may also broadcast a signal to a group of STAR lines.

SYNC100

Is used to synchronize multiple devices with respect to a given rising edge of CLK100 in order to provide very tight time coordination between modules. SYNC100 is distributed from Slot 0 to slots 1-12, with individual backplane buffers for each slot. A Slot 0 module implementing the SYNC100 function must provide an arbiter to synchronize external events to CLK100 that meets the guaranteed setup and hold times for the SYNC100 signal. This guarantees that all affected modules will trigger on the same CLK100 clock edge. SYNC100 is nominally a 10 ns pulse and may be initiated by any type of external or internal event.

VXI Address Space Definition

VXI assigns non-conflicting portions of the VME bus address space to its devices. 256 devices may exist in a VXI system and are referred to by logical device addresses 0 through 255. The VXI bus system configuration space is the upper 16k of the 64k A16 address space. Each device is granted a total of 64 bytes in this space.

If a device needs more space a dynamic memory assignment is performed at power-on. The "resource manager" reads the requirements and assigns the requested memory space by writing the module's new

VME bus address into the device's offset register. This method positions a device's additional memory space in the A24, A32, or A64 address space.

VXI bus Registers
VXI defines standard registers for use as configuration, communication and memory. VXI modules also have standard registers to provide manufacturer ID, Serial Number, Module Hardware / Firmware Revision Level.

The VXI bus specification defines further protocols, command and event formats and is supplemented by additional standards such as VXI plug & play to simplify it's use.

CERN VME 430 / "Nuclear VME" Standard

In order to make the VME bus suitable for data acquisition systems in nuclear and high energy physics experiments and to standardize used electronic equipment the European Physics Laboratory CERN developed in 1990 several VME crate specifications. These standards defined the VME crate design; mechanics, power supply and cooling.

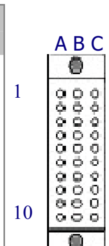
CERN VME crates were a modular designed, consisting of a VME bin with backplane and card cage with plug-in fan tray and power supply. This modularity made it easy to quickly exchange failing fan trays and power supplies.

The CERN **V422** standard described a 21 slot standard VME (VME64) crate. The **V430 "VME 430 - nuclear VME"** specification used a modified backplane to add bus lines and DC voltages needed for data acquisition applications.

As of today the original V422/V430 crates are not produced anymore however, there are still many modules and VME crates available and in use, which comply with the VME430 backplane.

The VME 430 backplane is a monolithic 6U backplane with 3 connector rows J1/Jaux/J2. Both J1 and J2 are outfitted with 3-row DIN-96pin type connectors with standard VME pinouts. This provides backwards compatibility, i.e. any standard VME / VME64 module will work in a CERN VME 430 compliant crate. The CERN VME 430 backplane adds a third dataway and connector row Jaux. Jaux was added in the middle between J1 and J2 to provide additional pins for DC power, geographic addressing and 3 differential bussed signals (clocks / timing).

Pin No.	Jaux/Paux (middle)		
	Row A	Row B	Row C
01	SN1	GND	SN2
02	SN3	GND	SN4
03	SN5	GND	GND
04	CK*	GND	CK
05	SG*	GND	SG
06	CL*	GND	CL
07	-2 V	-2 V	-2 V
08	- 15 V	CE	+ 15 V
09	- 5,2 V	-5,2 V	- 5,2V
10	- 5,2 V	- 5,2 V	- 5,2V



30-pin DIN 41612

CERN V430 Jaux Pin Layout

CE - Clean Earth
Un-bussed line without termination

CK - Clock signal
Is a bussed differential line terminated on both sides of the backplane (2 resistors to ground and 1 resistor in between the two lines according to the impedance).

CK positive logic /
CK* negative logic

CL - Clear
Is a bussed differential line terminated like CK lines.

CL positive logic
CL* negative logic

Geographical address
VME430 provides geographical addressing on the Jaux connector via SN1... SN5. The addresses are binary coded according to the slot numbers as shown in the following table (NC = No Connection represents H- level and can be generated by 5k6 resistor on VME module for TTL, e.g.):

Slot	SN1	SN2	SN3	SN4	SN5
01	NC	GND	GND	GND	GND
02	GND	NC	GND	GND	GND
03	NC	NC	GND	GND	GND
04	GND	GND	NC	GND	GND
05	NC*	GND	NC	GND	GND
06	GND	NC	NC	GND	GND
...	...	...	...	...	...
20	GND	GND	NC	GND	NC
21	NC	GND	NC	GND	NC

Geographic address coding

SG - Start / Stop Gate
Is a bussed differential line terminated like CK lines for timing applications:

SG positive logic
SG* negative logic

VME 430 DC / Power Supply Requirements
In addition to the regular VME DC voltages of 5V and +/-12V the CERN VME 430 specifies also –5.2V and –2V (for fast ECL logic) as well as optionally +/-15V. These voltages are supplied via the Jaux/Paux connectors. VME430 compliant modules often require these voltages for proper operation and may not function in a standard VME crate.

+5V, +/-12V (as per VME spec.),
-5.2V, -2V (for ECL devices / termination),
+/-15V (optional, for analog circuits)

VME Fan tray / cooling
A front side plug-in fan tray provides air flow for VME module cooling. The air temperature increase shall not exceed 10C. The fan tray has to be equipped with a fan fail detection system, which issues on a fan fail a local and remote warning and also can shut down the DC.

CERN Monitoring and Remote Control
According to the CERN V 430 specification for remote control and monitoring the following signal lines are available at a monitoring and control connector (CANON Type DAC 15-S-FO), which is placed at the bin backside

Line	Description
STATUS	status monitor output
FAN FAILURE	fan failure output
A.C.POWER INHIBIT	remote on / off
SYSRESET	manual system reset
0V SIGNAL	common control return line
DISABLE	global trip-off disable input
GND	ground

CERN V430 remote control & monitoring signals

STATUS and FAN FAILURE are switched by relay contacts. In correct operation, they are close to the return lines. The system-reset circuit is activated by a short circuit between the SYSRESET and the GND signal line. For trouble shooting purposes the global trip-off can be disabled by a jumper connection between INHIBIT and 0V SIGNAL lines.

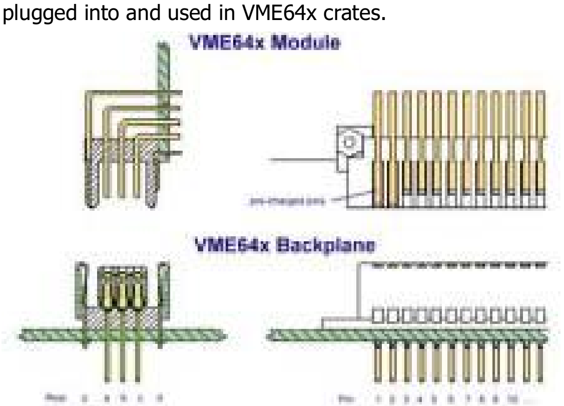
ANSI / VITA VME64x Standard

In 1997 the VITA Standards Organization (VSO) adopted a superset to the VME64 standard called the VME64 Extensions (VITA 1.1, VME64x). VME64x adds new features and capabilities such as:

- A new 160 pin connector family.
- A 95 pin P0/J0 connector.
- 3.3 V power supply pins.
- More +5 VDC power supply pins.
- Geographical addressing.
- Higher bandwidth (up to 160 Mbytes/sec).
- 141 more user-defined I/O pins.
- Rear plug-in units (transition modules).
- Live insertion / hot-swap capability.
- Injector / ejector locking handles.
- EMC (Electro Magnetic Compatible) front panels.
- ESD (Electrostatic Discharge) features.

Backplane

The main and obvious difference is the use of new 160-pin connectors, which are backwards compatible to the "old" 96-pin DIN connector. The 3 row "core" is identical to the VME/VME64 specification. All new bus and power lines are routed to the outer "z" and "d" rows. This makes all legacy VME and VME64 modules forward compatible to VME64x backplanes and sub-racks; i.e. these modules can be plugged into and used in VME64x crates.



VME64x 5-row connectors

The reverse of plugging a VME64x module into an older VME backplane or crate is mechanically possible however, will work only if the VME64x module does not make use of the 3.3VDC power. Further none of the new VME64x features as geographic addressing live insertion, or 64 bit transfer widths would be available. The monolithic backplane PCB must include both J1 and J2 connectors.

The VME64x standard also adds a new metric style P0/J0 connector in the middle between the top and bottom connectors. All pins except the outer rows (GND) are feed-through connections for I/O. The P0 connector is optional on the backplane.

IEEE1101.10 Mechanics

With VME64x new card rail and front panel mechanics with enhanced EMC/EMD features according to the IEEE 1101.10 standard are used:

- Front panel with guiding and coding pins, EMC strip
- Card guides with ground ESD clips
- Injector / ejector locking handles
- EMC strips on chassis

The new EMC style front panels/handles can have incompatibilities with older VME card cages outfitted according to the CERN VME430 standard.

Pin Assignment for the VME64x P1/J1 Connector					
Pin	**Row z**	**Row A**	**Row B**	**Row C**	**Row d**
1	MPR	D00	BBSY*	D08	VPC
2	GND	D01	BCLR	D09	GND
3	MCLK	D02	ACFAIL*	D10	+V1
4	GND	D03	BG0IN*	D11	+V2
5	MSD	D04	BG0OUT*	D12	RsvU
6	GND	D05	BG1IN*	D13	-V1
7	MMD	D06	BG1OUT*	D14	-V2
8	GND	D07	BG2IN*	D15	RsvU
9	MCTL	GND	BG2OUT*	GND	GAP*
10	GND	SYSCLK	BG1IN*	SYSFAIL*	GA0*
11	RESP*	GND	BG3OUT*	BERR*	GA1*
12	GND	DS1*	BR0*	SYSRESET*	+3.3V
13	RsvBus	DS0*	BR1*	LWORD*	GA2*
14	GND	WRITE*	BR2*	AM5	+3.3V
15	RsvBus	GND	BR3*	A23	GA3*
16	GND	DTACK*	AM0	A22	+3.3V
17	RsvBus	GND	AM1	A21	GA4*
18	GND	AS*	AM2	A20	+3.3V
19	RsvBus	GND	AM3	A19	RsvBus
20	GND	IACK*	GND	A18	+3.3V
21	RsvBus	IACKIN*	SERA	A17	RsvBus
22	GND	IAOUT*	SERB	A16	+3.3V
23	RsvBus	AM4	GND	A15	RsvBus
24	GND	A07	IRQ7*	A14	+3.3V
25	RsvBus	A06	IRQ6*	A13	RsvBus
26	GND	A05	IRQ5*	A12	+3.3V
27	RsvBus	A04	IRQ4*	A11	LI/I*
28	GND	A03	IRQ3*	A10	+3.3V
29	RsvBus	A02	IRQ2*	A09	LI/O*
30	GND	A01	IRQ1*	A08	+3.3V
31	RsvBus	-12 V	+5V STDBY	+ 12 V	GND
32	GND	+5 V	+ 5 V	+ 5 V	VPC

P1/J1 Pin Layout (row ABC identical to VME/VME64)

Pin Assignment for the VME-64x P2/J2 Connector					
Pin	**Row z**	**Row a**	**Row b**	**Row c**	**Row d**
1	UsrDef	UsrDef	+5 VDC	UsrDef	UsrDef
2	GND	UsrDef	GND	UsrDef	UsrDef
3	UsrDef	UsrDef	RETRY*	UsrDef	UsrDef
4	GND	UsrDef	A24	UsrDef	UsrDef
5	UsrDef	UsrDef	A25	UsrDef	UsrDef
6	GND	UsrDef	A26	UsrDef	UsrDef
7	UsrDef	UsrDef	A27	UsrDef	UsrDef
8	GND	UsrDef	A28	UsrDef	UsrDef
9	UsrDef	UsrDef	A29	UsrDef	UsrDef
10	GND	UsrDef	A30	UsrDef	UsrDef
11	UsrDef	UsrDef	A31	UsrDef	UsrDef
12	GND	UsrDef	GND	UsrDef	UsrDef
13	UsrDef	UsrDef	+5 VDC	UsrDef	UsrDef
14	GND	UsrDef	D16	UsrDef	UsrDef
15	UsrDef	UsrDef	D17	UsrDef	UsrDef
16	GND	UsrDef	D18	UsrDef	UsrDef
17	UsrDef	UsrDef	D19	UsrDef	UsrDef
18	GND	UsrDef	D20	UsrDef	UsrDef
19	UsrDef	UsrDef	D21	UsrDef	UsrDef
20	GND	UsrDef	D22	UsrDef	UsrDef
21	UsrDef	UsrDef	D23	UsrDef	UsrDef
22	GND	UsrDef	GND	UsrDef	UsrDef
23	UsrDef	UsrDef	D24	UsrDef	UsrDef
24	GND	UsrDef	D25	UsrDef	UsrDef
25	UsrDef	UsrDef	D26	UsrDef	UsrDef
26	GND	UsrDef	D27	UsrDef	UsrDef
27	UsrDef	UsrDef	D28	UsrDef	UsrDef
28	GND	UsrDef	D29	UsrDef	UsrDef
29	UsrDef	UsrDef	D30	UsrDef	UsrDef
30	GND	UsrDef	D31	UsrDef	UsrDef
31	UsrDef	UsrDef	GND	UsrDef	GND
32	GND	UsrDef	+5 VDC	UsrDef	VPC

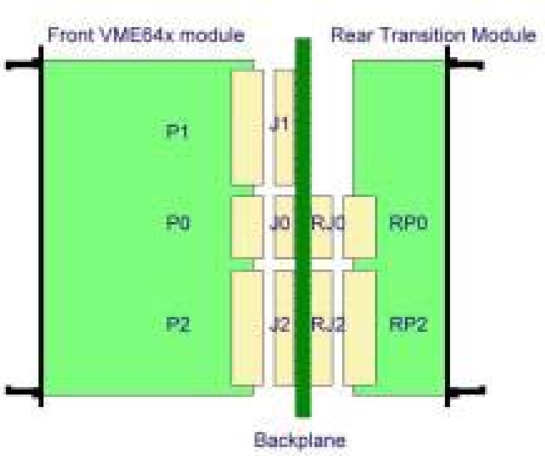
P2/J2 Pin Layout (row ABC identical to VME/VME64)

Pin Assignment for the VME64x P0/J0/RJ0/RP0 Connector						
Pin	Row f	Row e	Row d	Row c	Row b	Row a	Row z
1	GND	UD	UD	UD	UD	UD	GND
2	GND	UD	UD	UD	UD	UD	GND
3	GND	UD	UD	UD	UD	UD	GND
4	GND	UD	UD	UD	UD	UD	GND
5	GND	UD	UD	UD	UD	UD	GND
6	GND	UD	UD	UD	UD	UD	GND
7	GND	UD	UD	UD	UD	UD	GND
8	GND	UD	UD	UD	UD	UD	GND
9	GND	UD	UD	UD	UD	UD	GND
10	GND	UD	UD	UD	UD	UD	GND
11	GND	UD	UD	UD	UD	UD	GND
15	GND	UD	UD	UD	UD	UD	GND
16	GND	UD	UD	UD	UD	UD	GND
17	GND	UD	UD	UD	UD	UD	GND
18	GND	UD	UD	UD	UD	UD	GND
19	GND	UD	UD	UD	UD	UD	GND

P0/J0 Pin Layout

Transition Card Cage

For I/O a rear side card cage can house 6U x 80mm transition modules (101.11 rear I/O transition board standard). These use the feed-through pins of J0/RJ0 and J2/RJ2 to connect to the front side VME64x modules.



VME64x front and rear card/connector scheme

DC Voltages

In addition to the standard VME voltages (+5V, +/-12V) VME64x provides +3.3V. Two optional voltages V1 and V2 can be defined and used (mostly for +48V). Additional pins are foreseen for +5V (VPC) and Ground.
The resulting maximum power per board can be up to 200W with a total of 4kW per crate. This may require high performance power supplies and efficient, temperature controlled cooling.

Geographic Addressing

VME64x introduces 6 Geographic Addressing pins GA(4:0)*, GAP* on the J1/P1 d row allowing modules to be addressed by their slot (Geographically). This can replace the switches or jumpers that define base addresses on older VME modules. In order to be compatible to legacy VME bus systems VME64x may have both geographic and switch selectable base addressing.

Live Insertion

The VME64x standard also meets High Availability and Live Insertion (Hot Swap) standards. In combination with Geographic Addressing this makes it possible to remove and insert modules without shutting down the crate and supports automatically recognizing and configuring the modules in a "plug and play" way.

Increased Bandwidth

VME64x defines new protocols that increase the bandwidth of the parallel VME bus. The 2eVME protocol allows peak block data rate of up to 160 MB/sec by using master and slave terminated two-edge handshaking for each VME transfer.

A further improvement was introduced with 2eSST (VME 320 / VITA 1.5-2003), which defines a synchronous data strobe mode and achieves 320 Mbyte/s bandwidth.

These new protocols have to be implemented in the master and slave modules. The VME crate must be outfitted with a backplane capable of high-speed data transfers. All WIENER VME64x crates are tested for 2eVME and 2eSST transfers.

Topology	Bus Cycle	Maximum Speed
VMEbus / IEEE-1014	BLT	40 Mbyte/sec
VME64	MBLT	80 Mbyte/sec
VME64x	2eVME	160 Mbyte/sec
VME64x /VME320	2eSST	320 — 500+ Mbyte/sec

VME64xP - VIPA

In 1998, the "**V**ME-bus **I**nternational **P**hysics **A**ssociation" defined an extension for VME64x for use in nuclear and high energy physics experiments. This standard, VITA 23 (see also DOE/SC-0013 "Designer and User Guide"), uses a 9U x 400mm card size and defines some user-defined pins of the VME64x connector.

Further VME64xP adds 4 more DC voltages (Vw, Vx, Vy, Vz), which can be defined by the user. These should be used for low voltages as –2V or –5.2V. The VME64x V1 and V2 voltages should be used for +48V to power on board dc-to-dc converter.

VME64xP introduced the CBLT (chained Block Transfer) and MCST (multi cast writes). These modes allow consecutive read-out of several adjacent modules with one large block transfer. The end of the CBLT cycle is indicated by a BERR, which has to be processed accordingly by the VME master.

As of today the VME64xP standard is only used in a few applications however the CBLT and MCST protocols can be used on regular VME64x bus systems if they have a CBLT compatible backplane. WIENER VME64x backplanes can be ordered CBLT capable.

Pin Assignment for the VME64xP / VIPA P0/J0/RJ0/RP0 Connector							
Pin	Row f	Row e	Row d	Row c	Row b	Row a	Row z
01	COM	+5V	+5V	+5V	+5V	+5V	COM
02	COM	RET_WX	UD	+5V	TBUS1+	TBUS1-	COM
03	COM	RET_WX	UD	UD	TBUS2+	TBUS2-	COM
04	COM	Vw	UD	user I/O	user I/O	user I/O	COM
05	COM	Vw	UD	user I/O	user I/O	user I/O	COM
06	COM	RET_WX	UD	user I/O	user I/O	user I/O	COM
07	COM	AREF_WX	UD	user I/O	user I/O	user I/O	COM
08	COM	RET_WX	UD	user I/O	user I/O	user I/O	COM
09	COM	Vx	UD	user I/O	user I/O	user I/O	COM
10	COM	Vx	UD	user I/O	user I/O	user I/O	COM
11	COM	Vy	UD	user I/O	user I/O	user I/O	COM
12	COM	Vy	UD	user I/O	user I/O	user I/O	COM
13	COM	RET_YZ	UD	user I/O	user I/O	user I/O	COM
14	COM	AREF_YZ	UD	user I/O	user I/O	user I/O	COM
15	COM	RET_YZ	UD	user I/O	user I/O	user I/O	COM
16	COM	Vz	UD	user I/O	user I/O	user I/O	COM
17	COM	Vz	UD	UD	Tbus3+	Tbus3-	COM
18	COM	RET_yz	UD	UD	Tbus4+	Tbus4-	COM
19	COM	RET_yz	UD	UD	Tbusoc1	Tbusoc2	COM

ANSI / VITA VXS Standard

“VME-bus switched serial” VXS is a new ANSI / VITA standard which combines the 32-bit parallel VME-bus with high speed switched serial interconnect fabrics in order to increase the data transfer bandwidth to several GB/s.

VITA 41 / VXS was approved in May 2006 and consist of the base standard ANSI/VITA 41.0-2006 and additional, layered sub-specifications. VXS offers the following enhancements and new features:

- Standardized multi-GB/s switched serial interconnects to the parallel bus VME bus
- Standard open technology for the serial switched links
- Payload Modules with high speed differential RT2 connectors at J0/P0
- Switch modules with high-speed differential RT connectors (no VME J1/J2!)
- Additional D.C. power onto each VME module
- Backward compatibility with VME/VME64x

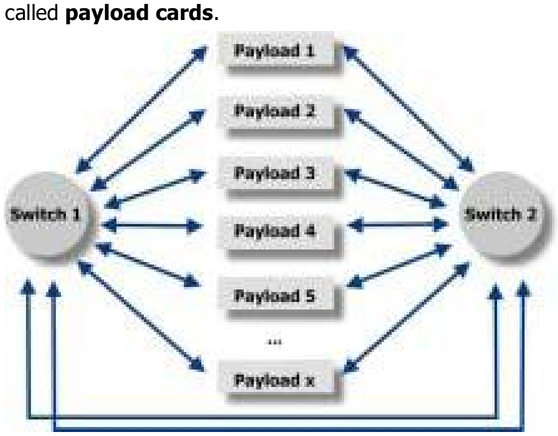
VITA 41.0 VXS provides the following specifications

VXS.0: base specification for mechanics, power, switch slot and payload card definitions
VXS.1: InfiniBand™ 4X link technology specification
VXS.2: Serial RapidIO™ 4X link technology specification
VXS.3: 1/10 Gigabit Ethernet technology
VXS.4: PCI Express 4X technology
VXS.5: Aurora Link 4X technology
VXS.6: 1 Gigabit Ethernet Control Channel Layer
VXS.7: Redundant Processor Mesh
VXS.10: Live Insertion Specification
VXS.11: Rear transition module Specification

Switch Fabric Architecture

VXS defines an interconnected network (fabric) of switched serial input and output ports with point-to-point connection with differential signals. An active switching device manages data transfers from inputs to outputs. For VXS all active switching devices are located on a special **switch card**. Depending on the VXS backplane size and configuration one or two switch card slots may be used.

All other modules that connect to the switch cards are called **payload cards**.



Dual Star configuration example

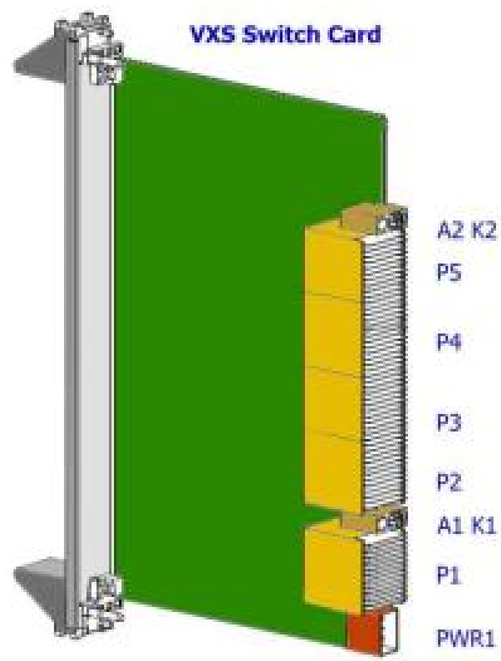
The switch fabric architecture supports connections from every payload card to one or two switch cards in a star, dual star or mesh topology. The availability of 2 switch boards supports redundant connections for high availability applications. This centralized switching scheme uses 16 pairs of differential signals, which are assigned, each pair is a bi-directional serial port. Ports can be used in parallel (trunked) for higher performance.

Switch Cards

A VXS compliant chassis can have one or two switch cards which have point-to-point connections to all payload cards. and allow all or a subset of the payload boards connected to it to intercommunicate.

Switch slots/boards are 6U x 160mm and have a new connector setup with 5 high speed MultiGig RT connectors (Tyco: 1410421-1, 1410137-1, 1410138-1 and 1410139-1 types for P1-P5) which is not compatible to the “VME P1/P2”. The lower P1 is defined as sideband connector for lower speed signals provides sideband communication between boards in the chassis.

Further switch cards are outfitted with a special, dedicated power connector (PWR1) and keying/alignment (A1-2, K1-2). The top rear above A2 and K2 is for user defined I/O. Switch cards shall conform to the VITA 41.10 live insertion standard.



The following tables show the pin assignment for the pairs of differential connections. The actual pin usage is defined in the appropriate protocol layer definition.

Switch Board P5 Connector						
	L/K	J/I	H/G	F/E	D/C	B/A
01	GND	D5-3-/+	GND	D5-2-/+	GND	D5-1-/+
02	D5-6-/+	GND	D5-5-/+	GND	D5-4-/+	GND
03	GND	D5-9-/+	GND	D5-8-/+	GND	D5-7-/+
04	D5-12-/+	GND	D5-11-/+	GND	D5-10-/+	GND
05	GND	D5-15-/+	GND	D5-14-/+	GND	D5-13-/+
06	D5-18-/+	GND	D5-17-/+	GND	D5-16-/+	GND
07	GND	D5-21-/+	GND	D5-20-/+	GND	D5-19-/+
08	D5-24-/+	GND	D5-23-/+	GND	D5-22-/+	GND
09	GND	D5-27-/+	GND	D5-26-/+	GND	D5-25-/+
10	D5-30-/+	GND	D5-29-/+	GND	D5-28-/+	GND
11	GND	D5-33-/+	GND	D5-32-/+	GND	D5-31-/+
12	D5-36-/+	GND	D5-35-/+	GND	D5-34-/+	GND
13	GND	D5-39-/+	GND	D5-38-/+	GND	D5-37-/+
14	D5-42-/+	GND	D5-41-/+	GND	D5-40-/+	GND
15	GND	D5-45-/+	GND	D5-44-/+	GND	D5-43-/+
16	D5-48-/+	J/I	D5-47-/+	GND	D5-46-/+	GND

Switch Board P4 Connector						
	L/K	J/I	H/G	F/E	D/C	B/A
01	GND	D4-3-/+	GND	D4-2-/+	GND	D4-1-/+
02	D4-6-/+	GND	D4-5-/+	GND	D4-4-/+	GND
03	GND	D4-9-/+	GND	D4-8-/+	GND	D4-7-/+
04	D4-12-/+	GND	D4-11-/+	GND	D4-10-/+	GND
05	GND	D4-15-/+	GND	D4-14-/+	GND	D4-13-/+
06	D4-18-/+	GND	D4-17-/+	GND	D4-16-/+	GND
07	GND	D4-21-/+	GND	D4-20-/+	GND	D4-19-/+
08	D4-24-/+	GND	D4-23-/+	GND	D4-22-/+	GND
09	GND	D4-27-/+	GND	D4-26-/+	GND	D4-25-/+
10	D4-30-/+	GND	D4-29-/+	GND	D4-28-/+	GND
11	GND	D4-33-/+	GND	D4-32-/+	GND	D4-31-/+
12	D4-36-/+	GND	D4-35-/+	GND	D4-34-/+	GND
13	GND	D4-39-/+	GND	D4-38-/+	GND	D4-37-/+
14	D4-42-/+	GND	D4-41-/+	GND	D4-40-/+	GND
15	GND	D4-45-/+	GND	D4-44-/+	GND	D4-43-/+
16	D4-48-/+	J/I	D4-47-/+	GND	D4-46-/+	GND

Switch Board P3 Connector						
	L/K	J/I	H/G	F/E	D/C	B/A
01	GND	D3-3-/+	GND	D3-2-/+	GND	D3-1-/+
02	D3-6-/+	GND	D3-5-/+	GND	D3-4-/+	GND
03	GND	D3-9-/+	GND	D3-8-/+	GND	D3-7-/+
04	D3-12-/+	GND	D3-11-/+	GND	D3-10-/+	GND
05	GND	D3-15-/+	GND	D3-14-/+	GND	D3-13-/+
06	D3-18-/+	GND	D3-17-/+	GND	D3-16-/+	GND
07	GND	D3-21-/+	GND	D3-20-/+	GND	D3-19-/+
08	D3-24-/+	GND	D3-23-/+	GND	D3-22-/+	GND
09	GND	D3-27-/+	GND	D3-26-/+	GND	D3-25-/+
10	D3-30-/+	GND	D3-29-/+	GND	D3-28-/+	GND
11	GND	D3-33-/+	GND	D3-32-/+	GND	D3-31-/+
12	D3-36-/+	GND	D3-35-/+	GND	D3-34-/+	GND
13	GND	D3-39-/+	GND	D3-38-/+	GND	D3-37-/+
14	D3-42-/+	GND	D3-41-/+	GND	D3-40-/+	GND
15	GND	D3-45-/+	GND	D3-44-/+	GND	D3-43-/+
16	D3-48-/+	J/I	D3-47-/+	GND	D3-46-/+	GND

Switch Board P2 Connector						
	L/K	J/I	H/G	F/E	D/C	B/A
01	GND	D2-3-/+	GND	D2-2-/+	GND	D2-1-/+
02	D2-6-/+	GND	D2-5-/+	GND	D2-4-/+	GND
03	GND	D2-9-/+	GND	D2-8-/+	GND	D2-7-/+
04	D2-12-/+	GND	D2-11-/+	GND	D2-10-/+	GND
05	GND	D2-15-/+	GND	D2-14-/+	GND	D2-13-/+
06	D2-18-/+	GND	D2-17-/+	GND	D2-16-/+	GND
07	GND	D2-21-/+	GND	D2-20-/+	GND	D2-19-/+
08	D2-24-/+	GND	D2-23-/+	GND	D2-22-/+	GND
09	GND	D2-27-/+	GND	D2-26-/+	GND	D2-25-/+
10	D2-30-/+	GND	D2-29-/+	GND	D2-28-/+	GND
11	GND	D2-33-/+	GND	D2-32-/+	GND	D2-31-/+
12	D2-36-/+	GND	D2-35-/+	GND	D2-34-/+	GND
13	GND	D2-39-/+	GND	D2-38-/+	GND	D2-37-/+
14	D2-42-/+	GND	D2-41-/+	GND	D2-40-/+	GND
15	GND	D2-45-/+	GND	D2-44-/+	GND	D2-43-/+
16	D2-48-/+	J/I	D2-47-/+	GND	D2-46-/+	GND

Switch Board P1 Connector								
	H	G	F	E	D	C	B	A
01	SYS RST*	SYS FAIL*	AC FAIL*	+5V STBY	SERB	SERA	RFU	PEN*
02	S1-16	LI/I	GAP*	GA4*	GA3*	GA2*	GA1*	GA0*
03	S1-24	S1-23	S1-22	S1-21	S1-20	S1-19	S1-18	S1-17
04	S1-32	S1-31	S1-30	S1-29	S1-28	S1-27	S1-26	S1-25
05	S1-40	S1-39	S1-38	S1-373	S1-363	S1-35	S1-34	S1-33
06	S1-48	S1-47	S1-46	S1-453	S1-443	S1-43	S1-42	S1-41
07	S1-56	S1-55	S1-54	S1-533	S1-523	S1-51	S1-50	S1-49
08	S1-64	S1-63	S1-62	S1-613	S1-603	S1-59	S1-58	S1-57
09	S1-72	S1-71	S1-70	S1-693	S1-683	S1-67	S1-66	S1-65
10	S1-80	S1-79	S1-78	S1-773	S1-763	S1-75	S1-74	S1-73
11	S1-88	S1-87	S1-863	S1-853	S1-843	S1-83	S1-82	S1-81
12	S1-96	S1-95	S1-94	S1-93	S1-92	S1-91	S1-90	S1-89
13	S1-104	S1-103	S1-102	S1-101	S1-100	S1-99	S1-98	S1-97
14	S1-112	S1-111	S1-110	S1-109	S1-108	S1-107	S1-106	S1-105
15	S1-120	S1-119	S1-118	S1-117	S1-116	S1-115	S1-114	S1-113
16	S1-128	S1-127	S1-126	S1-125	S1-124	S1-123	S1-122	S1-121

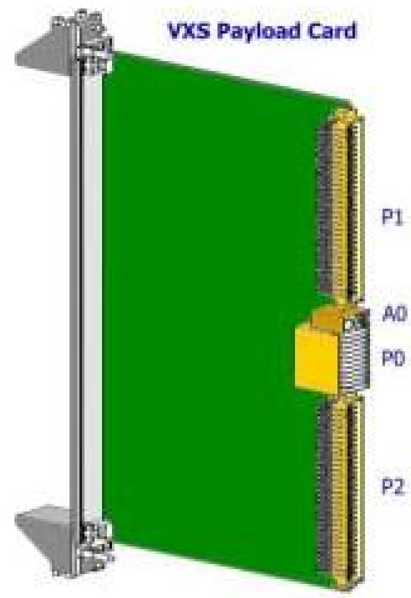
To provide DC to the switch board a 6-pin power connector (type Positronic PWR-6P-R, 10A current/pin rated) is used with the following pin assignment :

Pin 1: **VPC**
Pin 2-4: **+5V**
Pin 5-6: **GND**

Payload Cards

Payload cards are outfitted with VME P1 and P2 connectors as well as with a new high-speed connector for switched serial at the P0 position. Payload cards can use the VME bus only, both the VME bus and switched serial lines or only use the switched serial interconnects.

The VME-bus connectors P1 and P2 are as specified in the VME64x standard 5-row 160-pin connectors with identical pin layout (see VME64x section). All board mechanics as front panels and handles have to comply with IEEE 1101.10 (ESD / EMC enhanced).



The high-speed P0 connector (Tier 2, 7-Row, Tyco 1410147-1) has both differential pairs (DP) as well as single ended (SE) and ground (GND) lines. The individual pin usage depends on the implemented switched technology and is given in the protocol layer standards.
From the remaining P0 pins, one pin is defined to support live insertion (PEN*). Other pins are reserved for Future Use (RFU).

Payload P0 Pin layout							
	G	F	E	D	C	B	A
01	SE1	GND	DP2-	DP2+	GND	DP1-	DP1+
02	GND	DP4-	DP4+	GND	DP3-	DP3+	GND
03	SE2	GND	DP6-	DP6+	GND	DP5-	DP5+
04	GND	DP8-	DP8+	GND	DP7-	DP7+	GND
05	RFU	GND	RFU	RFU	GND	RFU	RFU
06	GND	RFU	RFU	GND	RFU	RFU	GND
07	RFU	GND	RFU	RFU	GND	RFU	RFU
08	GND	RFU	RFU	GND	RFU	RFU	GND
09	RFU	GND	RFU	RFU	GND	RFU	RFU
10	GND	RFU	RFU	GND	RFU	RFU	GND
11	PEN*	GND	RFU	RFU	GND	RFU	RFU
12	GND	DP24-	DP24+	GND	DP23-	DP23+	GND
13	SE7	GND	DP26-	DP26+	GND	DP25-	DP25+
14	GND	DP28-	DP28+	GND	DP27-	DP27+	GND
15	SE8	GND	DP30-	DP30+	GND	DP29-	DP29+

Each payload card is outfitted with one keying (K0) and alignment (A0) pin receptacle.

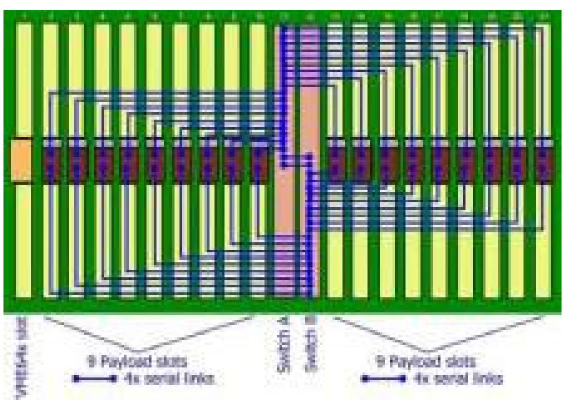
VXS Backplane

A 19" sub rack can hold a backplane with a maximum configuration of 18 payload slots and 2 switch slots. Backplanes with fewer payload or switch slots are allowed and can be configured in different topologies.

The VXS backplane design depends on the switch fabric topology, which can be one of:

- **Star:** each of up to 18 payload cards connects to a single switch card, no redundancy
- **Dual Star:** each of up to 18 payload cards connects to two separate switch cards, switch cards are interconnected, provides redundancy, most common configuration
- **Mesh:** each payload card is directly connected to every other card, with the 2 available ports up to 3 cards can be connected in a mesh without using a switch, used only on small backplanes
- **Daisy Chain:** each payload card is connected to its nearest neighbors, no switch is required however low (shared) bandwidth and limited reliability

In a Dual Star configuration the VXS backplane requires two switch cards and a maximum of 18 payload cards resulting in a maximum of 20 slots. However, a standard VME64x slot can be added to get a full size 21-slot backplane.



21-slot VXS backplane

VXS Power and Cooling

ANSI/VITA 1.7-2003 increased the maximum allowed currents for the 96 pin & 160 pin DIN/IEC connectors from the original 1A to 2A per pin. This allows higher crate power supply currents, and consequently higher power dissipation on the VXS boards which will be needed to fully utilize the high performance switch fabric capabilities.

This requires a better-designed chassis with improved ventilation that can adequately cool the higher power VXS boards. All WIENER crates can provide maximum DC power and are outfitted with high efficiency temperature controlled and monitored cooling fans.

VXS Layered Switch Fabric Standards

InfiniBand (VITA 41.1): with data rates of 16 Gb/s per 4x link, full duplex is designed for servers with ultra-high bandwidth. Infiniband operates at 2.5 Gb/s per pair.

Serial RapidIO (VITA 41.2): is a new high-speed serial physical layer using the "old" parallel RapidIO protocol. RapidIO is designed for communications inside a system rather than between systems. Serial RapidIO operates at 1.25 Gb/s, 2.5 Gb/s, or 3.125 Gb/s per pair. VITA 41.2 draft standard supports data rates of up to 20 Gbps per 4x link, full duplex.

Gigabit Ethernet (VITA 41.3): Gigabit Ethernet is a well-established serial protocol. VITA 41.3 supports data rates of up to 8 Gb/s per 4x link, full duplex.

PCI Express (VITA 41.4): PCI Express has been selected by the PCI-SG as the next generation successor to the PCI bus. PCI Express operates at 3.125 Gb/s per pair. The VXS VITA 41.4 draft standard supports data rates of up to 20 Gb/s per 4x link, full duplex.

WIENER VME/VXI/VXS crate configurations and options

WIENER crates feature a modular design so that we can provide any required configuration of mechanics, backplanes or power supply based on standard WIENER components and parts.

9U VME-430 6023 crate example:

1) UEL6020 EX fan tray with combo interface, plugged in from front
2) Optional air dust filter
3) 1U Plenum chamber for homogeneous air distribution (6023 style)
4) Optional Vario divider with 6 slots 6Ux160mm
5) Optional J3 backplane
6) Optional rear side card cage
7) UEP 6021 power supply plugged in from rear

WIENER VME / VXI / VXS Products:

- Powered crates
- VME Controllers
- VME modules